

AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1 Claim 1 (currently amended) A circuit for generating an output phase signal with
2 a ~~an~~ variable phase shift relative to a reference phase, including
3 an oscillator outputting phase signals at n outputs, each of which is shifted in
4 phase by $\varphi = 360^\circ/n$ from one output to the next and is correspondingly
5 staggered in time relative to each other by Δt ,
6 a first multiplexer, the inputs of which are connected to the even-number outputs
7 of the oscillator and which passes on to its output a phase signal output by an
8 output x of the oscillator as a function of a first phase selection signal output by a
9 phase select circuit, where x is a selected one of the n outputs of the oscillator
10 ~~determined by the phase output signal to be generated,~~
11 a second multiplexer, the inputs of which are connected to the odd-number
12 outputs of the oscillator and which passes to its output on a phase signal output
13 by an output x + 1 of the oscillator as a function of a second phase selection
14 signal output by the phase select circuit,
15 a phase interpolator receiving the phase signals output by the multiplexers and
16 controlling with these the periodic opening and closing of a first set of phase
17 switches in the time spacing of Δt ,
18 the phase interpolator containing a first charging circuit in which a charging
19 voltage of a capacitor is varied by switching current sources assigned to the first
20 set of phase switches on or off in accordance with the closing or opening of the
21 first set of phase switches,
22 whereby a number of current sources is provided corresponding to the number of
23 interphase shift values to be generated between the phase shifts of the phase
24 signals output by the first and second multiplexers ~~determined by the phase~~
25 ~~select signal,~~ to each of which at least two phase switches are assigned, of
26 which the one in each case is controlled by the phase signal output by the first

27 multiplexer and the other by the phase signal output by the second multiplexer, a
28 first set of separating switches ~~switch~~ being inserted in the connection between
29 each of the phase switches and the assigned current source_i;
30 characterized in that
31 in each connection between each phase switch and the charging circuit a second
32 set of separating switches ~~switch~~ is inserted,
33 and that a control circuit (SS1-SS32) is provided which ensures that the first set
34 of separating switches (TR1a to TR32a, TR1b to TR32b) assigned to each
35 phase switch (PS1a-1 to PS1a-32, PS1b-1 to PS1b-32) and the second set of
36 separating switches (TR1a-1 to TR1a-32, TR1b-1 to TR1b-32) assigned to the
37 same phase switch are never open at the same time when there is a change in
38 the phasing of the ~~output~~ phase signal output by the circuit relative to the
39 reference phase.

1 Claim 2 (currently amended) The circuit in claim 1, characterized in that a
2 second charging circuit (L2) is provided, that parallel to each phase switch a
3 second set of phase switches ~~switch~~ (PS2a-1 to PS2a-32, PS2b-1 to PS2b-32) is
4 arranged which can be switched opposite in phase to that of the assigned phase
5 switch, and that in the connection between the second phase switch in each
6 case and the second charging circuit a further set of separating switches ~~switch~~
7 (TR2a-1 to TR2a-32 ~~TR2-32~~, TR2b-1 to TR2b-32 ~~TR2-32~~) is inserted in each
8 case which is signaled equal in phase to the first and second sets of separating
9 switches located between a current source and the first charging circuit (L1),
10 resulting in a second output phase signal (V2) being producible from the second
11 charging circuit (L2) which is phase-shifted by 180° relative to the output phase
12 signal (V1) generated by the first charging circuit (L1).